REMARKS

By this amendment, claims 1, 13, 15, 19, and 22 have been amended. Accordingly, claims 1-6 and 8-25 are pending in the present application. The claim amendments are supported by the specification, the accompanying figures, and claims as originally filed, with no new matter being added. In particular, support for the amendments can be found in Figures 9-15 of the application as filed. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

In addition, Applicants have amended the specification to remove objected to language and to recite: "the second terminus being located below capacitor cell dielectric layer 44 and between the ~~upper and lower surfaces of, or within, [within]~~ lower bulk insulator layer 36." Support for this amendment can be found in Figures 9-15 of the application as filed. The drawings are an integral part of the disclosure of the invention and the specification can be amended to recite that which is shown in the drawings. MPEP 8th ed. § 2163.06 ("[I]nformation contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter."). The Examiner's acceptance of the foregoing amendments to the specification are therefore respectfully requested.

1. Rejection of the Amendment to the Specification

The Examiner has objected to various amendments to the specification entered in the Amendment and Response filed April 2, 2002 under 35 U.S.C. § 132. In particular, the Examiner has interpreted the "terminus" of the recited sleeve insulator layer to be the horizontal end portion of the sleeve insulator layer that is coplanar with the cell plate insulating layer. The Examiner has therefore objected to the language that describes the first terminus as "substantially adjacent to cell plate layer 46," and language variations thereof. Applicants respectfully traverse.

In order to further the prosecution of this application, the specification has been amended to remove each reference to the first terminus being "substantially adjacent to cell plate layer 46," and language variations thereof. Accordingly, Applicants respectfully request the prompt removal of the foregoing objection.

2. Rejections Under 35 U.S.C. § 112

Claims 1-6 and 8-22 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. In particular, the Examiner has rejected the claims due to the phrase "a first terminus adjacent to the conductor layer." Applicants respectfully traverse.

This language has been deleted from the claims in order to further the prosecution of this case. Accordingly, the prompt removal of this rejection under 35 U.S.C. § 112, first paragraph is respectfully requested.

3. Rejections Under 35 U.S.C. § 102

Claims 1-6, 8-10, and 12-21 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,165,839 to Lee et al (hereinafter "*Lee*"). Applicants respectfully traverse.

Present independent claims 1, 13, and 15 recite, *inter alia*, with language variations in each claim: "a sleeve insulator layer in contact with the conductor layer, the sleeve insulator layer comprising: a first terminus; and a second terminus opposite the first terminus, the second terminus located between the upper and lower surfaces of the lower bulk insulator."

Lee has no such disclosure. Rather, *Lee* discloses a silicon nitride spacer 26 on the side of a bit line contact hole, adjacent a top silicon nitride layer 22 at a first terminus, adjacent an interlayer

dielectric layer 21 and a cell plate structure, and having a second terminus coplanar to a silicon nitride layer 10 at the top of a lower bulk insulator layer 9. (Figure 15). Thus, in contrast to the present claims, *Lee* does not disclose a second terminus "located between the upper and lower surfaces of the lower bulk insulator."

Present independent claim 19 recites, *inter alia,* "the sleeve insulator layer comprising . . . the second terminus separated from the semiconductor substrate and in contact with the capacitor storage node." In contrast, *Lee* does not disclose that the sleeve insulator layer, let alone the second terminus, is "in contact with the capacitor storage node."

Accordingly, for at least the above reasons, Applicants submit that claims 1, 13, 15, and 19, as well as dependent claims 2-6, 8-10, 12, 14, 16-18, and 20-21 are not anticipated by *Lee.* Applicants therefore respectfully request that the rejection of claims 1-10 and 12-21 under 35 U.S.C. §102(e) over *Lee* be withdrawn.

Claims 1-6, 8-10, and 13-18 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,973,910 to Gardner (hereinafter "*Gardner*") for the reasons set forth on page 3 of the Office Action. Applicants respectfully traverse.

Present independent claims 1, 13, and 15 recite, *inter alia*, with language variations in each claim: "a sleeve insulator layer in contact with the conductor layer, the sleeve insulator layer comprising: a first terminus; and a second terminus opposite the first terminus, the second terminus located between the upper and lower surfaces of the lower bulk insulator."

Gardner discloses, in contrast, a structure in which the sidewall insulator 107 extends to the top of substrate 100 at a second terminus (Figure 2). *Gardner* therefore clearly does not disclose "the second terminus located between the upper and lower surfaces of the lower bulk insulator."

Further, Applicants note that claims 1, 13, and 15 also recite that the conductive contact or

plug extends beyond the sleeve insulator layer to terminate at a contact on the substrate whereas *Gardner* discloses that insulator 107 and conductive contact 108 both terminate at the surface of substrate 100.

Accordingly, Applicants submit that claims 1-6, 8-10, and 13-18 are not anticipated by *Gardner*. Applicants therefore respectfully request that the rejection of these claims under 35 U.S.C. §102(e) over *Gardner* be withdrawn.

Claims 19-21 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,475,247 to Kim (hereinafter "*Kim*") for the reasons set forth on page 3 of the Office Action. Applicants respectfully traverse.

Kim is directed to a manufacturing process for providing a contact structure, and discloses an insulating layer 15' on the sidewall of a contact hole used as the storage electrode (although the disclosure in *Kim* is vague, it appears that layer 16 in Fig. 2G is the storage electrode 16). *Kim* depicts the insulating layer 15' as having a first terminus adjacent the top edge of a third dielectric layer 13, which is disposed over a second dielectric layer 9, which overlies a capacitor cell plate conductor layer 8 and an insulator 7.

In contrast, present independent claim 19 recites, *inter alia*, "an electrically conductive plug in contact with the active region and the storage node; and a sleeve insulator layer insulating the capacitor cell plate from the electrically conductive plug." *Kim* does not disclose either of these limitations. First, *Kim* does not disclose a plug in contact with the active region (3') and the storage node (16). Second, *Kim* does not disclose a sleeve insulator layer insulating the capacitor cell plate from the electrically conductive plug because it insulates the capacitor cell plate 8 from the storage node 16.

Accordingly, Applicants respectfully assert that claims 19-21 are not anticipated by *Kim*.

Applicants therefore respectfully request that the rejection of these claims under 35 U.S.C. § 102(b) be withdrawn.

4. Rejections Under 35 U.S.C. § 103(a)

Claims 11 and 12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Gardner* in view of U.S. Patent No. 5,338,700 to Dennison et al. (hereinafter "*Dennison*") and U.S. Patent No. 6,198,143 B1 to Ohsaki (hereinafter "*Ohsaki*") for the reasons set forth on pages 4-5 of the Office Action. Applicants respectfully traverse.

Claims 11 and 12 depend from claim 1, and thus include contain the limitations thereof. As previously discussed, claim 1 recites, *inter alia*: "a sleeve insulator layer in contact with the conductor layer, the sleeve insulator layer comprising: a first terminus; and a second terminus opposite the first terminus, the second terminus located between the upper and lower surfaces of the lower bulk insulator" and "a conductive contact extending from and beyond the sleeve insulator layer to terminate at a contact on said semiconductor substrate." There is no teaching or suggestion in *Gardner* of these recitations in present claim 1. Rather, *Gardner* discloses that insulator 107 has a second terminus and a conductive contact 108 that both terminate at the surface of substrate 100.

Dennison and *Ohsaki* cannot overcome the foregoing deficiencies of claim 1. Thus, even if the teachings of these cited references are combined, not all of the limitations of claims 11 and 12 would be met. Accordingly, Applicants submit that claims 11 and 12 would not have been obvious over the cited references. Applicants therefore respectfully request that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn.

Claims 22-25 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of *Ohsaki* for the reasons set forth on pages 5-6 of the Office Action. Applicants respectfully

traverse.

Present independent claim 22 recites, *inter alia*, "an electrically insulating layer formed conformably upon the conductor layer . . . the sleeve insulator layer comprising: a first terminus adjacent to and in contact with the electrically insulating layer [conductor layer]; and a second terminus opposite the first terminus, the second terminus above the semiconductor substrate and within the lower bulk insulator layer."

Lee has no teaching or suggestion of these recitations of present claim 22 for several reasons. First, Figure 15 of *Lee* discloses that spacers 26 have a first terminus and a second terminus, the first terminus located coplanar with a silicon nitride layer 22 that overlies the interlayer dielectric layer 21, which in turn overlies the conductor layer 20. *Lee* therefore teaches a different structure than the presently recited claim 22, which recites: "a first terminus adjacent to and in contact with the electrically insulating layer." As recited in claim 22, the electrically insulating layer is different from *Lee's* layer 22 because it is formed conformably upon the conductor layer. Next, *Lee* discloses the second terminus is coplanar with silicon nitride layer 10. *Lee* therefore does not teach or suggest, and provides no motivation to form, the presently recited: "a second terminus above the semiconductor substrate and within the lower bulk insulator layer."

Ohsaki does not disclose a sleeve insulator layer and therefore cannot overcome the above limitations of *Lee*. Thus, even if the teachings of *Lee* and *Ohsaki* are combined, not all of the limitations of claim 22 and dependent claims 23-25 would be met. Therefore, Applicants submit that claims 22-25 would not have been obvious over the cited references. Applicants therefore respectfully request that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the present claims. In the event the Examiner finds any remaining impediment to the prompt allowance of this application that could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 17th day of October 2002.

Respectfully submitted,

William J. Athay
Attorney for Applicants
Registration No. 44,515

WORKMAN, NYDEGGER & SEELEY
1000 Eagle Gate Tower
60 East South Temple
Salt Lake City, Utah 84111
Telephone: (801) 533-9800
Fax: (801) 328-1707

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VERSION WITH MARKINGS SHOWING THE CHANGES MADE

In The Specification:

Please replace the paragraph beginning at page 11, line 7 with the following rewritten paragraph:

-- Referring to Figure 9, a second etch step, which is anisotropic, is carried out to remove substantially all of the horizontally-exposed portions of sleeve insulator layer 50 from the bottom of the partially formed BLCC. Sleeve insulator layer 50 thus covers the exposed portions of capacitor cell dielectric layer 44, cell plate layer 46, and cell plate insulating layer 48 that are within contact hole 70. As illustrated in Figure 9, sleeve insulator layer 50 thus has a first terminus substantially adjacent to [cell plate layer 46 and] cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and between the upper and lower surfaces of, or within, [within] lower bulk insulator layer 36.--

Please replace the paragraph beginning at page 14, line 17 with the following rewritten paragraph:

--Referring to Figure 14, a circle 80 illustrates in phantom a cross-section of an etch hole through upper bulk insulator layer 51. A center line 80 represents an axis passing through the center of circle 80. In Figure 14, center line 71 represents the axis passing through the center of sleeve insulator layer 50. The symbol Δ_3 represent the misalignment from the center of circle 80 to the center of sleeve insulator layer 50. As with sleeve insulator layer 50 in Figure 9, sleeve insulator layer 50 in Figure 14 has a first terminus substantially adjacent to [cell plate layer 46 and] cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and between the upper and lower surfaces of, or within, [within]lower bulk insulator layer 36.--

Please replace the paragraph beginning at page 15, line 15 with the following rewritten paragraph:

-- The process creating the structure seen in Figure 14 is substantially the same as that creating the structure seen in Figure 15. In Figure 15, a circle 90 illustrates in phantom a cross-section of an etch hole through upper bulk insulator layer 51. The etch hole is aligned with respect to sleeve insulator layer 50. As with sleeve insulator layer 50 in Figure 9, sleeve insulator layer 50 in Figure 15 has a first terminus substantially adjacent to [cell plate layer 46 and] cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and between the upper and lower surfaces of, or within, [within]lower bulk insulator layer 36. Also, the etch is self aligned with sleeve insulator layer 50 due to the selectivity of the etch with respect to the material from which sleeve insulator layer 50 is substantially composed, and due to the etch selectivity to the material of which cell plate insulating layer 48 is composed. As was described with respect to Figure 13, the self-alignment of the etch through sleeve insulator layer 50 in effect assures electrical insulation of cell plate layer 46 to prevent an electrical short with electrically conductive bit line contact 92 within the BLCC. Figure 15 illustrates the maximum contact size on active area 18b, as dictated by the

diameter of the area defined within sleeve insulator layer 50. Electrical insulation protection of bit line contact 92 is provided by cell plate insulating layer 48 and sleeve insulator layer 50 so as to prevent shorting of cell plate layer 46 with bit line contact 92.--

Please replace the paragraph beginning at page 16, line 3 with the following rewritten paragraphs:

--Figure 16 shows the divergent types of contacts that can be made using the invention, although all of the depicted contacts need not be present in the same structure nor be situated as depicted in Figure 16. In Figure 16, circle 90 illustrates in phantom a cross-section of an etch hole, made by conventional etch processes, through upper bulk insulator layer 51. A contact plug 72 in upon source/drain region 18b. Electrically conductive bit line contact 92 is situated within contact hole 70 and passes through sleeve insulator layer to terminate upon contact plug 72. As with sleeve insulator layer 50 in Figure 9, sleeve insulator layer 50 in Figure 16 has a first terminus substantially adjacent to [cell plate layer 46 and] cell plate insulating layer 48. Sleeve insulator layer 50 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and between the upper and lower surfaces of, or within, [within]lower bulk insulator layer 36.

Circle 94 illustrates in phantom a cross-section of a contact hole 98, made by conventional etch processes, through upper bulk insulator layer 51 and into a transistor stop on a gate 24 beneath an insulating protective layer 28 of a transistor. Electrically conductive contact 100 is situated within contact hole 98 and passes through a sleeve insulator layer 52 to make contact with gate 24. Sleeve insulator layer 52 in Figure 16 has a first terminus substantially adjacent to [cell plate layer 46 and] cell plate insulating layer 48. Sleeve insulator layer 52 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44, between the upper and lower surfaces of, or within, [within]lower bulk insulator layer 36, and in contact with storage node layer 42.

Circle 104 illustrates in phantom a cross-section of a contact hole 106, made by conventional etch processes, through upper bulk insulator layer 51 and into storage node layer 42. Electrically conductive contact 102 is situated within contact hole 106 and passes through a sleeve insulator layer 53 to make contact with storage node layer 42. Sleeve insulator layer 53 insulates electrically conductive contact 102 from cell plate layer 46. Sleeve insulator layer 53 in Figure 16 has a first terminus substantially adjacent to [cell plate layer 46 and] cell plate insulating layer 48. Sleeve insulator layer 53 also has a second terminus opposite the first terminus, the second terminus being located below capacitor cell dielectric layer 44 and in contact with storage node layer 42.--

In the claims:

Claims 1, 13, 15, 19, and 22 have been amended as follows:

1. (Thrice Amended) A contact structure for an integrated circuit comprising:

a lower bulk insulator layer situated above a semiconductor substrate, the lower bulk insulator having upper and lower surfaces;

a conductor layer situated above the lower bulk insulator layer;

a sleeve insulator layer in contact with the conductor layer, the sleeve insulator layer comprising:

a first terminus [adjacent to the conductor layer]; and

a second terminus opposite the first terminus, the second terminus located between the upper and lower surfaces of the lower bulk insulator [above the semiconductor substrate and within the lower bulk insulator layer]; and

a conductive contact extending from and beyond the sleeve insulator layer to terminate at a contact on said semiconductor substrate, said conductive contact being ~~electrically insulated from the conductor layer by the sleeve insulator layer~~.

13. (Thrice Amended) A contact structure for an integrated circuit comprising:

a lower bulk insulator layer situated above a semiconductor substrate, the lower bulk insulator having upper and lower surfaces;

a conductor layer situated above the lower bulk insulator layer;

an upper bulk insulator layer upon the conductor layer;

a sleeve insulator layer in contact with the conductor layer, the sleeve insulator layer comprising:

a first terminus [adjacent to the conductor layer] and

a second terminus opposite the first terminus, the second terminus located between the upper and lower surfaces of the lower bulk insulator [above the semiconductor substrate and within the lower bulk insulator layer]; and

a conductive plug extending from and beyond the sleeve insulator layer to terminate at a contact on said semiconductor substrate, said conductive plug being electrically insulated from the conductor layer by the sleeve insulator layer.

15. (Thrice Amended) A contact structure for an integrated circuit comprising:

a lower bulk insulator layer situated above a semiconductor substrate, the lower bulk insulator layer having upper and lower surfaces and a sidewall;

a dielectric layer situated above the lower bulk insulator layer;

a conductor layer situated above the lower bulk insulator layer and above the dielectric layer, the conductor layer having a sidewall;

an electrically insulating layer situated upon the conductor layer;

a sleeve insulator layer in contact with the lower bulk insulator layer sidewall and the conductor layer sidewall, the sleeve insulator layer comprising:

a first terminus [adjacent to the conductor layer]; and

a second terminus opposite the first terminus, the second terminus located between the upper and lower surfaces of the lower bulk insulator [above the semiconductor substrate and within the lower bulk insulator layer]; and

a conductive plug extending from and beyond the sleeve insulator layer to terminate at a contact on said semiconductor substrate, said conductive plug being electrically insulated from the conductor layer by the sleeve insulator layer.

19. (Thrice Amended) A contact structure for an integrated circuit comprising:

a semiconductor substrate having an active region therein;

a capacitor storage node in contact with the active region;

a capacitor dielectric upon the capacitor storage node;

a capacitor cell plate upon the capacitor dielectric;

an electrically conductive plug in contact with the active region and the storage node; and

a sleeve insulator layer insulating the capacitor cell plate from the electrically conductive plug, the sleeve insulator layer in contact with the capacitor storage node, the capacitor dielectric, and the capacitor cell plate, the sleeve insulator layer comprising:

a first terminus [adjacent to the capacitor cell plate]; and

a second terminus opposite the first terminus, the second terminus separated from [above] the semiconductor substrate and in contact with the capacitor storage node.

22. (Thrice Amended) A contact structure for an integrated circuit comprising:

a lower bulk insulator layer situated above a semiconductor substrate;

a dielectric layer above the lower bulk insulator layer;

a conductor layer situated above the dielectric layer;

an electrically insulating layer formed conformably upon the conductor layer;

a sleeve insulator layer comprising a material selected from the group consisting of Ta_2O_5 and Si_3N_4, the sleeve insulator layer comprising:

a first terminus adjacent to and in contact with the electrically insulating layer [conductor layer]; and

a second terminus opposite the first terminus, the second terminus above the semiconductor substrate and within the lower bulk insulator layer; and

a conductive contact terminating at a refractory metal silicide material contact on said semiconductor substrate and being electrically insulated from the conductor layer by the sleeve insulator layer.